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RONALD P KANANEN
RADER FISHMAN & GRAUER
THE LION BUILDING
1233 20TH STREET NW SUITE 501
WASHINGTON, DC 20036

EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/424,544	INO ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2006 & 22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,25-29,31,37 and 43-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,25-29,31,37 and 43-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings were received on 4 February 2004. These drawings are acceptable.

Information Disclosure Statement

3. The information disclosure statement filed 9 January 2006 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the proposed paper is unsigned by applicants' representative, Mr. Brian K Dutton (Reg. No. 47,255). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicants are advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 6, 25-29, 31, 37 and 43-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al (US 4,825,203 A) in view of Lee (US 5,426,447 A).

Regarding claim 6, Takeda discloses a liquid crystal display [Fig. 2, 11] comprising: a display portion in which a plurality of pixels [Fig. 2, 11-c] are two-dimensionally arranged at intersecting points of gate lines [Fig. 2, 11-a] as many as a plurality of rows and signal lines [Fig. 2, 11-b] as many as a plurality of columns which are wired in a matrix shape; a plurality of driver circuits [Figs. 1(A) & 2, 13 & q_1-q_n] for applying a signal potential to each pixel in said display portion through the signal lines of said plurality of columns (see Column 2, Line 56 - Column 3, Line 27); and time-divisional switches [Fig. 1(A), 32] for time-divisionally sending a signal

potential [Fig. 1(A), V_R, V_G & V_B] that is outputted from each of said plurality of driver circuits to the signal lines of said plurality of columns, characterized in that a time-dividing number of said time-divisional switches is equal to 3 [see Fig. 1(A), 32], the number of output terminals of each of said plurality of driver circuits is set to a measure [i.e. 1, for instance] of the total number [i.e. N] of signal lines of said plurality of columns, the number of output terminals of each of said plurality of driver circuits is set to a same number, when a size of a frame portion [Fig. 1(A), q_N] adjacent to said display portion is specified, the number [i.e. n = 1, for instance] of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion, when the total number of signal lines of said plurality of columns that is decided by a display system is set to N [Fig. 1(A), Q_1 to Q_N], the number of said driver circuits is set to N/n [Fig. 1(A), q_1 to q_N -- wherein N/1 = N], said total number of signal lines (N > 1) being different than said number (n = 1) of output terminals (see Column 4, Lines 22-68).

Although Takeda's Figures 1(A) and 2 render it readily apparent that the column electrode drive circuit [13] comprises driver ICs outside the display substrate [11], and although every material presently known to man possesses an inherent insulative capacity, and although it's arguable that the Takeda's LCD must feature at least one transparent substrate in order for a user to actually view a displayed image, Takeda does not expressly use the explicit term, "transparent insulating substrate" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion is formed (see Column 1, Lines 28-30).

Takeda and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Lee's transparent insulating glass substrate to form Takeda's liquid crystal display, so as to make it possible for users to actually view any displayed images.

Regarding claim 25, this claim is rejected by the reasoning applied in rejecting claim 6; furthermore, Takeda discloses a liquid crystal display [Fig. 2, 11] comprising: a display portion [Fig. 2, 11], said display portion having a plurality of gate lines [Fig. 2, 11-a], a plurality of signal lines [Fig. 2, 11-b] and a plurality of pixels [Fig. 2, 11-c], a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and a plurality of driver circuits [Figs. 1(A) & 2, 13, q_1-q_N], said plurality of driver circuits including at least one general driver circuit [Figs. 1(A), q_1 & q_2] and one remainder driver circuit [Figs. 1(A), q_n], each said at least one general driver circuit having a plurality of general driver circuit output terminals [Fig. 1(A), 36], a general driver circuit output terminal of said plurality of general driver circuit output terminals [Fig. 1(A), Q1 & Q2] providing a signal potential to one of said plurality of signal lines, said remainder driver circuit having a plurality of remainder driver circuit output terminals [Fig. 1(A), 36], a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines [Fig. 1(A), Q_N], the quantity [i.e. 2, for instance] of said remainder driver circuit output terminals being defined as (S - (OP * (DC-1))), "S" being the quantity [i.e. 5, for instance] of said plurality of signal lines, "OP" being the quantity [i.e. 3, for instance] of said general driver circuit output terminals, and "DC" being

the quantity [i.e. 2, for instance] of said plurality of driver circuits, and said quantity [i.e. 3] of said general driver circuit output terminals being different than said quantity [i.e. 2] of said remainder driver circuit output terminals [see Fig. 1(A) and Column 4, Lines 22-68 -- wherein S - (OP * (DC-1)) = 5 - (3 * (2-1)) = 5 - (3 * 1) = 5 - 3 = 2 = the quantity of remainder driver circuit output terminals = 2].

Takeda does not expressly use the explicit term, "pixel" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion comprising a plurality of "pixels" is formed (see Column 1, Lines 18-30).

Takeda and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Lee's "pixel" terminology to describe Takeda's "display picture elements", so as to make use of common terminology in the art.

Regarding claim 26, Takeda discloses each driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits [see Fig. 1(A)].

Regarding claim 27, Takeda discloses said plurality of pixels is arranged in a two-dimensional matrix shape (see Fig. 2).

Regarding claim 28, Takeda discloses said pixel of said plurality of pixels includes a transistor [Fig. 2, 11-d], a gate electrode [Fig. 2, at 11-a] of said transistor being electrically connected to said gate line, a source/drain [Fig. 2, at 11-b] of said transistor being electrically connected to said signal line (see Fig. 2; Column 2, Lines 56-68).

Regarding claim 29, Takeda discloses said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns (see Fig. 2).

Regarding claim 31, Takeda discloses a surplus connecting region [Fig. 2; 12, 13, & 15] that does not contribute to said display portion [Fig. 2, 11] does not occur on the said display (see Column 2, Line 56 - Column 3, Line 27).

Regarding claim 37, Takeda discloses an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch [Fig. 1(A), 32], said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line (see Column 4, Lines 22-68).

Regarding claim 43, Takeda discloses said plurality of primary colors is a first primary color, a second primary color and a third primary color (see Column 2, Lines 55-68).

Regarding claim 44, Takeda discloses said quantity [i.e. 3, for instance] of general driver circuit output terminals is greater than said quantity [i.e. 2, for instance] of remainder driver circuit output terminals [see Fig. 1(A)].

Regarding claim 45, Takeda discloses the sum total of general driver circuit output terminals [i.e. 3, for instance] and said remainder driver circuit output terminals [i.e. 2, for instance] is equal to said plurality of signal lines [i.e. 5, for instance] [see Fig. 1(A)].

Regarding claim 46, Takeda discloses said plurality of driver circuits include more than one said general driver circuit [see Fig. 1(A)].

Regarding claim 47, Takeda discloses each said general driver circuit has an equal number of general driver circuit output terminals [see Fig. 1(A)].

Regarding claim 48, Takeda discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (see Fig. 2; Column 2, Line 56 - Column 4, Line 6).

Regarding claim 49, this claim is rejected by the reasoning applied in rejecting claims 6 and 25; furthermore, Takeda discloses a liquid crystal display [Fig. 2, 11] comprising: a display portion [Fig. 2, 11], said display portion having a plurality of gate lines [Fig. 2, 11-a], a plurality of signal lines [Fig. 2, 11-b] and a plurality of pixels [Fig. 2, 11-c], a pixel of said plurality of

pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and a plurality of driver circuits [Figs. 1(A) & 2, 13 & q_1-q_n] (see Column 2, Line 56 - Column 3, Line 27), each of said plurality of driver circuits having a plurality of driver circuit output terminals [Fig. 1(A), at 37], a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line [Fig. 1(A), Q_1 to Q_N] of said plurality of signal lines, the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (see Column 4, Lines 22-68).

Takeda does not expressly use the explicit term, "pixel" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion comprising a plurality of "pixels" is formed (see Column 1, Lines 18-30).

Takeda and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Lee's "pixel" terminology to describe Takeda's "display picture elements", so as to make use of common terminology in the art.

Regarding claim 50, Takeda discloses a plurality of time-divisional switches [Fig. 1(A), 32], said plurality of time-divisional switches receiving said signal potential from said driver circuit output terminal and time-divisionally sending said received signal potential said signal line (see Column 4, Lines 22-68).

Regarding claim 51, Takeda discloses the quantity of said time-divisional switches is equal to 3 [see Fig. 1(A), 32] (see Column 4, Lines 22-68).

Regarding claim 52, Takeda discloses said quantity of said signal lines is different than said quantity of said driver circuit output terminals (see Fig. 1(A) and Column 4, Lines 22-68).

Regarding claim 53, Takeda discloses said quantity of said driver circuit output terminals is set to a power of 2 (see Fig. 1(A) and Column 4, Lines 22-68).

Regarding claim 54, although Takeda's Figures 1(A) and 2 render it readily apparent that the column electrode drive circuit [13] comprises driver ICs outside the display substrate [11], and although every material presently known to man possesses an inherent insulative capacity, and although it's arguable that the Takeda's LCD must feature at least one transparent substrate in order for a user to actually view a displayed image, Takeda does not expressly use the explicit term, "transparent insulating substrate" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion is formed (see Column 1, Lines 28-30).

Takeda and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary skill in the art

at the time of invention to use Lee's transparent insulating glass substrate to form Takeda's liquid crystal display, so as to make it possible for users to actually view any displayed images.

Regarding claim 55, Takeda discloses a memory circuit [Fig. 1(A), 31] for temporarily storing data [Fig. 1(A), D] to be written into said plurality of driver circuits; and a control circuit [Fig. 2, 15] for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit (see Column 3, Lines 8-27 & Column 4, Lines 22-68).

Regarding claim 56, Takeda discloses a leading waveform and a trailing waveform of a signal output waveform [Fig. 1(B), C_R, C_G & C_B] of each of said plurality of driver circuits are symmetrical with respect to a time base (see Column 4, Lines 47-68).

Regarding claim 57, Takeda discloses a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 58, Takeda discloses a leading time and a trailing time of each of said plurality of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 59, Takeda discloses a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal Scanning

period - the period of time selected by the time-divisional switches x 3) / 3 (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 60, Takeda discloses said plurality of driver circuits have a function to stop the operation of an output circuit of said plurality of driver circuits for said blanking period (see Fig. 1(B); Column 4, Line 22 - Column 5, Line 15).

Regarding claim 61, Takeda discloses said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) [see Fig. 1(A), V_R, V_G & V_B] by diving to said time-divisional switches (see Column 4, Lines 22-46).

Regarding claim 62, Takeda discloses within a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red [see Fig. 4(B); Row i+2 & Columns j, j+1 and j+2].

Regarding claim 63, Takeda discloses within a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue [see Fig. 5(B); Row i & Columns j, j+1 and j+2].

Regarding claim 64, Takeda discloses time-division of said time- division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel [see Figs. 4(A-B); Column 5, Lines 16-58].

Regarding claim 65, Takeda discloses a surplus connecting region [Fig. 2; 12, 13, & 15] that does not contribute to said display portion [Fig. 2, 11] does not occur on the said display (see Column 2, Line 56 - Column 3, Line 27).

Regarding claim 66, Takeda discloses said driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits [see Fig. 1(A)].

7. Claims 6 and 25 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al (US 4,745,406 A) in view of Lee (US 5,426,447 A).

Regarding claim 6, Hayashi discloses a liquid crystal display (see the Abstract) comprising: a display portion [Fig. 8; P] in which a plurality of pixels [Fig. 8, P] are two-dimensionally arranged at intersecting points of gate lines [Fig. 8, G] as many as a plurality of rows and signal lines [Fig. 1, L] as many as a plurality of columns which are wired in a matrix shape; a plurality of driver circuits [Fig. 8; 2 & 11] for applying a signal potential [Fig. 8; 1R, 1G, 1B] to each pixel in said display portion through the signal lines of said plurality of columns; and time-divisional switches [Fig. 8, 13R, 13G, 13B, 12, Ms] for time-divisionally sending a signal potential [Fig. 8; 1R, 1G, 1B] that is outputted from each of said plurality of driver circuits

to the signal lines of said plurality of columns, characterized in that a time-dividing number of said time-divisional switches is equal to 3 [Fig. 8, 13R, 13G, 13B] (see also Fig. 9), the number of output terminals of each of said plurality of driver circuits is set to a measure [i.e. 1, for instance] of the total number [e.g. 4] of signal lines of said plurality of columns, the number of output terminals of each of said plurality of driver circuits is set to a same number, when a size of a frame portion [Fig. 8, Ms] adjacent to said display portion is specified, the number [i.e. n = 1, for instance] of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion, when the total number of signal lines of said plurality of columns that is decided by a display system is set to N [e.g. 4], the number of said driver circuits is set to N/n [Fig. 8, Ms -- wherein N/1 = N], said total number of signal lines (N > 1) being different than said number (n = 1) of output terminals (see Column 4, Line 43 - Column 5, Line 8).

Although Hayashi's Figure 8 renders it readily apparent that the shift register [2] comprises driver ICs outside the display substrate [11], and although every material presently known to man possesses an inherent insulative capacity, and although it's arguable that the Hayashi's LCD must feature at least one transparent substrate in order for a user to actually view a displayed image, Hayashi does not expressly use the explicit term, "transparent insulating substrate" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion is formed (see Column 1, Lines 28-30).

Hayashi and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary

skill in the art at the time of invention to use Lee's transparent insulating glass substrate to form Hayashi's liquid crystal display, so as to make it possible for users to actually view any displayed images.

Regarding claim 25, this claim is rejected by the reasoning applied in rejecting claim 6; furthermore, Hayashi discloses a liquid crystal display (see the Abstract) comprising: a display portion [Fig. 8; P], said display portion having a plurality of gate lines [Fig. 8, G], a plurality of signal lines [Fig. 1, L] and a plurality of pixels [Fig. 8; P], a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and a plurality of driver circuits [Fig. 8; 2 & 11], said plurality of driver circuits including at least one general driver circuit [Fig. 8; Ms, Ms+1, Ms+2] and one remainder driver circuit [Figs. 8, Ms+3, Ms+4], each said at least one general driver circuit having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines, said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines, the quantity [i.e. 2, for instance] of said remainder driver circuit output terminals being defined as (S - (OP * (DC-1))), "S" being the quantity [i.e. 5, for instance] of said plurality of signal lines, "OP" being the quantity [i.e. 3, for instance] of said general driver circuit output terminals, and "DC" being the quantity [i.e. 2, for instance] of said plurality of driver circuits, - and said quantity [i.e. 3] of said general driver circuit output terminals being different than said

quantity [i.e. 2] of said remainder driver circuit output terminals [see Fig. 1(A) and Column 4, Line 43 - Column 5, Line 8 -- wherein S - (OP * (DC-1)) = 5 - (3 * (2-1)) = 5 - (3 * 1) = 5 - 3 = 2 = the quantity of remainder driver circuit output terminals = 2].

Hayashi does not expressly use the explicit term, "pixel" when describing the structure of the liquid crystal display.

However, Lee does disclose a transparent insulating substrate (e.g. glass) on which a display portion comprising a plurality of "pixels" is formed (see Column 1, Lines 18-30).

Hayashi and Lee are analogous art, because they are from the shared field of liquid crystal display device structures. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Lee's "pixel" terminology to describe Hayashi's "display picture elements", so as to make use of common terminology in the art.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 49 is further rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al (US 4,745,406 A).

Regarding claim 49, this claim is rejected by the reasoning applied in rejecting claims 6 and 25; furthermore, Hayashi discloses a liquid crystal display (see the Abstract) comprising: a display portion [Fig. 8; P], said display portion having a plurality of gate lines [Fig. 8, G], a

plurality of signal lines [Fig. 1, L and a plurality of pixels [Fig. 8; P], a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and a plurality of driver circuits [Fig. 8; 2 & 11], each of said plurality of driver circuits having a plurality of driver circuit output terminals [Fig. 8, 13R, 13G, 13B, 12, Ms], a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines, the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (see Column 4, Line 43 - Column 5, Line 8).

Reopening of Prosecution

10. In view of the 'Supplemental Appellant's Brief' filed on 17 August 2006, but mostly due to Applicants' submission of an information disclosure statement on 26 May 2005 (filed after the Final Office Action mailed 4 November 2003), PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth above.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee

can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Response to Arguments

11. Applicants' arguments filed 17 August 2006 and 4 February 2004 have been fully considered but they are not persuasive.

The examiner respectfully notes that over the course of the past three years of prosecution, the applicants' representative, Mr. Brian K Dutton (Reg. No. 47,255) has submitted three consecutive non-compliant Appeal Briefs. The latest Appeal Brief (filed 17 August 2006) is unfortunately yet again in a state of non-compliance -- due at least to faulty 'Status of Claims' and 'Status of Amendments' sections, both including a host of extraneous statements and information having little or nothing to do respectively with the current status of claims as well as amendments filed subsequent to final rejection.

The examiner further respectfully notes that each of the amendments submitted on 4 February 2004, 8 March 2004, and 22 July 2004 (and all after the final rejection mailed 4 November 2003) by the applicants' representative, Mr. Brian K Dutton (Reg. No. 47,255) were also non-compliant -- due at least to inaccurate status identifiers and improperly marked-up claim text amendments.

Additionally, Mr. Dutton failed to sign the information disclosure statement filed 9 January 2006.

MPEP § 1205.03 states, "The appeal will be dismissed if the appellant does not timely file an amended brief, or files an amended brief which does not overcome all the reasons for noncompliance of which the appellant was notified."

By all rightful USPTO policies and practices, as a result of Mr. Dutton's series of non-compliant submissions, the examiner has had four distinct and legitimate opportunities to officially abandon the instant application. As a courtesy to the applicants, the examiner has not done so. Furthermore, in an effort to the clear the air of an increasingly contentious prosecution, the examiner, as yet another courtesy to the applicants, has reopened prosecution -- incorporating the applicants' preferred claim constructions (in spite of their noncompliant nature) and addressing the applicants' concerns of any earlier applied prior art (which might still somewhat apply to the newly added/amended claims).

12. Applicants' arguments with respect to claims 6, 25-29, 31, 37, and 43-66 have been considered but are moot in view of the new grounds of rejection.

Due to the inclusion of the noncompliant claim amendments filed 4 February 2004, the applicants' arguments in the noncompliant Appeal Brief filed 17 August 2006 are no longer commensurate in scope with the current claim language.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ishizaki et al (5,748,171 A), Yajima et al (5,191,450 A), Morozumi (RE33,882 E), Yamamoto et al (4,801,933 A), Hayashi et al (4,745,406 A), Morozumi (4,716,403 A), and Morozumi (4,600,274 A) are cited to further evidence the state of the art pertaining to liquid crystal displays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Piziali
27 November 2006

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600